Amendments to the Specification

Please replace the paragraph beginning on page 1, lines 12-22, as follows:

Programmable logic devices (PLDs), such as field programmable gate arrays (FPGAs) and the like, are well known. A programmable logic device comprises a complex logical element that may be programmed to effect combinational logic, sequential logic, or combined combination and sequential logic functions. Thus, a PLD allows for software modifications of sequential and/or combinational logic in a physical layer. In this manner, bug fixes, feature enhancements, and other improvements to systems incorporating PLDs may be provided via software update.

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Please replace the paragraph beginning on page 2, lines 7-16, as follows:

The disadvantages associated with the prior art are overcome by the present invention of an apparatus and method for programming a remote programmable logic device. In a first embodiment, the apparatus comprises a processing system having a first file to second file conversion program stored therein.~~[[;]]~~ ~~the~~ The processing system receives ~~receiving~~ the first file from a first communications medium and transmits ~~transmitting~~ the converted second file through a second communications medium in a format native to the remote programmable logic device.

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Please replace the paragraph beginning on page 2, line 27 to page 3, line 3, as follows:

In a second embodiment, the apparatus for programming at least one programmable logic devices comprises at least one circuit board respectively comprising the at least one programmable logic device coupled to at least one switching circuit. A processor system is coupled to the at least one switching circuit via a board select bus and a JTAG bus, wherein the processor system executes a file in a format native to the at least one programmable logic device. The native format file enables the at least one switching circuit via the board select bus, and then programs the at least one programmable logic device via the JTAG bus.

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Please replace the paragraph beginning on page 4, lines 15-26, as follows:

The processor system 120 includes a processor board 122 and an Ethernet port 138. The Ethernet port 138 is in communication with the remote source of programming data 110, such as a computer workstation or personal computer, via a network 112, such as local area network (LAN) or wide area network (WAN) denoted as LAN/WAN 112, and illustratively an Ethernet link. Furthermore, the processor board 122 comprises various components coupled to a bus 132 including at least one processor (e.g., a CPU) 124, a buffer 126, memory [[ ]](e.g., RAM) 128, and support circuits 130. The memory 128 stores software (i.e., File/JTAG conversion program 150) for performing a file/JTAG conversion method 200 (FIG. 2).

Please replace the paragraph beginning on page 5, lines 15-25, as follows:

Moreover, by utilizing the JTAG physical layer directly within the back plane of a multi-board or multi-module system, the number of pins within the back plane connections may be reduced. That is, rather than having discrete pins or electrical connections made to each of a plurality of boards, modules, or sub-systems including field programmable gate arrays, a single set of contacts or signal paths adhering to the physical layer and related protocols described in IEEE Standard 1149.1 may be used to effect reprogramming operations on each of the plurality of boards, modules, or sub-systems included within the system.

Please replace the paragraph beginning on page 5, line 26 to page 6, line 3, as follows:

FIG. 2 depicts a flow diagram of a method 200 for programming one or more remote programmable logic devices ~~440~~ 142 according to the invention. The method 200 begins in step 202 and proceeds to step 204 where a programmer or technician accesses the remote programming workstation 110 and inputs program code in a first file format native to the programming workstation 110. For example, the program code may be written in a program language such as microcode from ALTERA®, or the like. The program code may also be generated automatically according to a rules-based

a6 ~~epert~~ expert system in response to configuration changes or ~~ethe rsystem~~ other system changes, upgrades, and the like.

Please replace the paragraph beginning on page 8, lines 6-15, as follows:

a7 FIG. 3 depicts a high-level block diagram of an information processing system including apparatus according to an embodiment of the invention. Specifically, FIG. 3 depicts an interactive information distribution system 300 such as a video information distribution system. Such a system is described in more detail in U.S. patent ~~application Serial~~ No. 6,166,730 ~~09/322,814~~, entitled "System For Interactively Distributing Information Services" ~~and filed October 14, 1999~~, which is incorporated herein by reference in its entirety as fully reproduced herein.

Please replace the paragraph beginning on page 8, lines 26-32, as follows:

a8 The remote programming source 310 is coupled to the HEC 320 via a first communications path 319, such as a telecommunications medium (e.g., LAN/WAN connection, Internet, or the like), or by a physical medium (e.g., CD- ROM 322, which is drawn in phantom). The head-end controller 320 is coupled to the server 330 via a second communications path 321 such as an Ethernet connection.

Please replace the paragraph beginning on page 9, line 33 to page 10, line 8, as follows:

a9 In one embodiment each circuit board 334 is physically coupled to the at least one processor 332 via a backplane 333. The backplane 333 may be a compact PCI backplane having n slots (not shown) for receiving the one or more circuit boards 334. A backplane suitable for use in the present invention is described in detail in U.S. patent ~~application Serial~~ No. 6,289,376 ~~09/363,670~~, entitled "Tightly-Coupled Disk-To-CPU Storage Server", ~~filed July 29, 1999,~~ which is hereby incorporated by reference herein as fully reproduced herein.

Please replace the paragraph beginning on page 10, line 24 to page 11, line 2, as follows:

FIGS. 4A and 4B together depict a relational flow diagram 400 between various functional elements of the information processing system 300 of FIG. 3. Generally, the head-end controller 320 receives via a first communications medium 319, a file having a format native to at least one programmable logic device 338. The head-end controller 320 sends the native format file to a processor system (e.g., server or switch) 330 via a second communications medium 321. The processor system 330 executes the native format file to identify and selectively access the at least one programmable logic device 338 via a first bus 340, and then programs the selectively accessed programmable logic devices 338 via a second bus 342.

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Please replace the paragraph beginning on page 11, lines 3-20, as follows:

In particular, the flow chart depicts a sequence of events, which are utilized to program a programmable logic device (PDL) such as the ROM in a field programmable gate array. The method 400 begins in step 402 where a programmer generates ~~an~~ a programmer object file (POF) on a remotely located workstation or personal computer. The POF is a compiled binary file. In step 404, a software conversion program (e.g., JAM file conversion software) having the capability to convert the POF into a file containing JAM byte code (JBC) is initiated by the programmer at the remote computer. The JAM conversion software is an executable program specific for a particular type of programmable logic device, which builds target files from source files (e.g., POF) by utilizing specific dependency and build specification rules. Specifically, the JAM software identifies target files, examines a file system to determine those targets requiring an update, and issues operating system (OS) ~~OS~~ commands to update such target files.

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Please replace the paragraph beginning on page 11, lines 21-26, as follows:

In step 406, the programmer transfers the JBC file to the head-end controller via a first communications path. The first communications path may be a

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telecommunications medium such as such as the Internet or any LAN/WAN networking channel. Alternately, the JBC file may be stored in a physical medium 332, such as tape, CD-ROM, and the like.

Please replace the paragraph beginning on page 12, lines 11-21, as follows:

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In step 418 the JBC program marks the identified target files (PDL's) by enabling the switching circuit 336 on the circuit board 334. Specifically, the JBC program marks the PLD target files that require an upgrade (i.e., reprogramming). Once the switching circuit 336 corresponding to the identified target files are set in an enabling mode, then, in step 420, the JBC program is transferred to the corresponding PLD's 338 requiring an update via the JTAG bus 342. Specifically, in step 422, the switching circuits 336 that have been enabled, transfer the JBC program from the processor board 332, via the JTAG bus 342, to the PLD 338.